APPARATUS AND METHOD FOR ASYNCHRONOUSLY INTERFACING HIGH-SPEED CLOCK DOMAIN AND LOW-SPEED CLOCK DOMAIN

ABSTRACT

Interfacing circuitry for asynchronously transferring data between a high-speed clock domain and a low-speed clock domain is provided. The interfacing circuitry is divided into halves, with one half being synchronized to a first clock and the second half being synchronized to a second clock. The first half and the second half are mirror images of each other. Each half has at least one storage component, such as a register and a flip-flop, for storing a valid bit as well as data, and at least one multiplexer component for gating the storage component. The valid bit is used to control the multiplexer at a receiving half. When transferring from a high-speed clock domain to a low-speed clock domain, the high-speed clock domain may probe the received data and/or the valid bit stored in the low-speed clock domain before the high-speed clock domain sends additional data.